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SILICIDE PROXIMITY STRUCTURES FOR CMOS DEVICE PERFORMANCE IMPROVEMENTS

Abstract

A method for manufacturing an integrated circuit having a plurality of semiconductor devices including an n-type field effect transistor and a p-type field effect transistor on a semiconductor wafer by creating a spacer having a first width for the n-type field effect transistor and creating a spacer having a second width for the p-type field effect transistor, the first width being greater than the second width and depositing silicide material on the semiconductor wafer such that tensile mechanical stresses are formed within a channel of the n-type field effect transistor and compressive stresses are formed within a channel of the p-type field effect transistor.